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Floor-plan and Routing Guidelines for High-speed Transmitters

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***Abstract*— Floor-planning and routing of high speed transmitters, which play major role in data transmission at very high rates, is becoming more complex with shrinking technology. Here we attempt to describe common guidelines for layout design, including experimental parasitic reduction techniques for drivers.**

I. Introduction

Layout design for high-speed transceivers such as USB, HDMI, SERDES, MPHY, etc is very challenging because of their high speed, huge switching currents, IR drop limitations and ESD guidelines. Improper floor-plan results in routing congestion, increased area leading to higher cost and parasitic effects which affect the performance of the modules.

As the technology shrinks, spacing between metal layers gets reduces, increasing the coupling capacitance between the signals. Since the dimensions of the devices and metals also reduces with shrinking technology, parasitic resistance increases and current carrying capacity decreases. The best practices in layout design to handle such issues have been discussed in this paper.

II. Floor-planning and routing guidelines

Usual transmitter architecture includes driver, pre-driver, reference voltage and current generators, digital logic circuits, clocking circuits, level-shifters and ESD (Electro Static Discharge) protection devices. One of the deciding factors in fixing the size of the module is pad size and number of pads used in the module. If the orientation of the module is in Y-direction then X-size is limited by pad size, distance between the pads and number of pads. Y-size is decided by estimating size of each sub-block in the module and by considering space for metal routing [1].

Location and direction of signal pins is decided by considering which block they interact with outside the module. Pins interacting with digital portion of the block should be in routing grids if the digital logic is constructed using physical design. If the pins are intended for the testing some signals then suitable location has to be identified for them.

Drivers and primary protection devices should be placed close to the pad to minimize IR drop. Sufficient space should be provided for metals since switching current is very high. Pre-drivers should be placed following the drivers. Current and voltage generators should be placed near to the blocks they are sourcing to.

If signals are of opposing directions, long run of such signals in same metal should be avoided to reduce coupling effect. As the device dimensions shrink in lower length technologies, the spacing between poly and the source and drain contacts reduces. This increases the miller capacitance. Different experiments have been done to reduce the miller capacitance by reducing source and drain contacts as shown in "Fig. 1" and the percentage reduction in capacitance has been tabulated in TABLE I. However this results in increase in IR drop. Hence reduction of contacts should be optimized to meet both constraints.

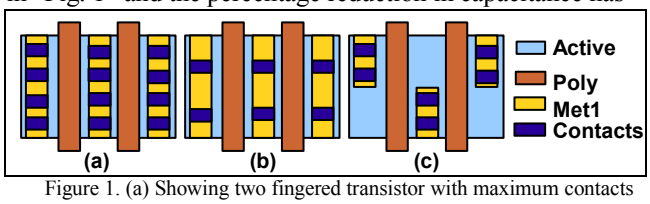

Figure 1. (a) Showing two fingered transistor with maximum contacts over source and drain. (b) showing reduced contacts by increasing spacing between them. (c) showing removal of contacts along with met1.

If there are multiple channels involved in transmitter,the parasitic capacitance of all of them should match each other. All the data and clock signals should be shielded properly to avoid coupling. The current sink section of the drivers should be arranged properly to minimize process variations. The ground connection should give equal resistances to all channels to avoid skew between data channels. Bias signals should not cross over any high-speed switching signals to avoid coupling. Power and ground routing should be laid out with minimum resistance by choosing higher metal levels and widths with kelvin connections to each block.

TABLE I. Experimental Results

Miller capacitance	**Percentage of reduction**	
	With contact reduction	***With contact and metal1 reduction***
	27.1%	34.60%

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